INSTITUTO POLITÉCNICO NACIONAL

SECRETARÍA ACADÉMICA

DIRECCIÓN DE EDUCACIÓN SUPERIOR

SYNTHESIZED SCHOOL PROGRAM

ACADEMIC UNIT: ESCUELA SUPERIOR DE CÓMPUTO

ACADEMIC PROGRAM: Ingeniería en Sistemas Computacionales.

LEARNING UNIT: Advanced FPGA Devices Programming **LEVEL:** III

AIM OF THE LEARNING UNIT:
The student implements advanced digital circuits based on field programmable logic devices.

CONTENTS:

I. FPGA architectures.
II. FPGA Application Analysis.
III. FPGA Application Design.
IV. Design simulation.
V. Design Synthesis and routing
VI. Performance analysis and debugging

TEACHING PRINCIPLES:

This learning unit will be addressed from project-oriented learning strategies, deductive and inductive methods with which to carry out learning activities that will guide the development of skills of abstraction, analysis and design of efficient algorithms; using theoretical and practical tools, such is the case of the embodiment circuit using a hardware description language (HDL) that demonstrate the concepts of the unit. The activities performed in class encourage the students some techniques, such as collaborative, participative, brainstorming, graphic organizers, documentary research, presentation of complementary topics, guided discussion and practical work in laboratory

EVALUATION AND PASSING REQUIREMENTS:

The program will evaluate the students in a continuous formative and summative way, which will lead into the completion of project portfolio. Some other assessing methods will be used, such as revisions, practical´s, class participation, exercises, learning evidences and a final project.

Other means to pass this Unit of Learning:

- Evaluation of previously acquired knowledge, with base in the issues defined by the academy.
- Official recognition by either another Academic Unit of the IPN or by a national or international external academic institution besides IPN.

REFERENCES:

- Cofer, R.C. (2006). *Rapid System Prototyping with FPGAs, Accelerating the Design Process*. UK: Elsevier-Newnes. ISBN: 978-0-7506-7866-7.
- Deschamps, J. P. (2006). *Synthesis of Arithmetic Circuits FPGA, ASIC, and Embedded Systems*. New Jersey: John Wiley & Sons, Inc. ISBN: 978-0471-68783-2.
- Ion, G. (2008). *Digital Systems Design with FPGAS*, UK: Elsevier-Newnes. ISBN-13: 978-0-7506-8397-5.
- Kilts, S. (2007). *Advanced FPGA Design Architecture, Implementation, and Optimization*. New Jersey: John Wiley & Sons, Inc. ISBN 978-0-470-05437-6.
- Pong, P. C. (2008). *FPGA Prototyping by VHDL examples*. New Jersey: John Wiley & Sons, Inc. ISBN: 978-0-471-72092-8.

INSTITUTO POLITÉCNICO NACIONAL

SECRETARÍA ACADÉMICA

DIRECCIÓN DE EDUCACIÓN SUPERIOR

ACADEMIC UNIT: Escuela Superior de Cómputo.

ACADEMIC PROGRAM: Ingeniería en Sistemas Computacionales.

FORMATION AREA: Professional.

MODALITY: Full-time.

LEARNING UNIT: Advanced FPGA Devices Programming.
TYPE OF LEARNING UNIT: Theoretical - Practical, Optative.
VALIDITY: August, 2012.
LEVEL: III.
CREDITS: 7.5 Tepic, 4.39 SATCA

ACADEMIC AIM

This learning unit contributes to the graduate profile of the Engineer in Computer Systems, to develop skills in digital systems design and computers architecture, using the application development process based on field programmable logic devices. It also develops strategic thinking, creative thinking, collaborative work and assertive communication.

This learning unit requires the knowledge acquired in the learning units Fundamentals of Digital Design, Design of Digital Systems and Computer Architecture, as well as the ability to describe an electronic circuit using a hardware description language for programming solutions on a programmable logic device (FPGA).

AIM OF THE LEARNING UNIT:

The student implements advanced digital circuits based on field programmable logic devices.

CREDITS HOURS

THEORETICAL CREDITS / WEEK: 3.0

PRACTICAL CREDITS / WEEK: 1.5

THEORETICAL HOURS / SEMESTER: 54

PRACTICAL HOURS / SEMESTER: 27

AUTONOMOUS LEARNING HOURS: 54

CREDITS HOURS / SEMESTER: 81

LEARNING UNIT DESIGNED BY:
Academia de Sistemas Digitales.

REVISED BY:
Dr. Flavio Arturo Sánchez Garfias.
Subdirección Académica

APPROVED BY:
Ing. Apolinar Francisco Cruz Lázaro.
Presidente del CTCE

AUTHORIZED BY: Comisión de Programas Académicos del Consejo General Consultivo del IPN

Ing. Rodrigo de Jesús Serrano Domínguez
Secretario Técnico de la Comisión de Programas Académicos

THEMATIC UNIT: I **TITLE:** FPGA architectures

UNIT OF COMPETENCE

The student analyzes the architecture of field programmable logic devices based on the type of technology used.

No.	CONTENTS	Teacher led-instruction HOURS		Autonomous Learning HOURS		REFERENCES KEY
		T	P	T	P	
1.1 1.1.1 1.1.2 1.1.3 1.1.4	Programmable logic devices GAL devices, PAL SPLD devices CPLD devices FPGA devices	0.5		2.0		3B
1.2 1.2.1 1.2.2 1.2.3 1.2.4	FPGA Architecture Logical Block Routing matrix and global signals Input and output blocks FPGA memory	0.5		2.0		
	Subtotals:	1.0		4.0		

TEACHING PRINCIPLES

This unit will be addressed from the strategy of collaborative learning and inductive teaching method, allowing the consolidation of the following learning techniques: documentary research, worksheet, concept maps, team exposition in complementary subjects.

LEARNING EVALUATION

Diagnostic evaluation
Portfolio of evidence:

Worksheet	10%
Conceptual map	5%
Teamwork	15%
Self-assessment rubrics	5%
Headings of co-evaluation	5%
Evidence of learning	60%

THEMATIC UNIT: II **TITLE:** FPGA Application Analysis

UNIT OF COMPETENCE

The student characterizes the steps involved in an application based on field programmable logic devices.

No.	CONTENTS	Teacher led-instruction HOURS		Autonomous Learning HOURS		REFERENCES KEY
		T	P	T	P	
2.1	Workloads	0.5		2.0	0.5	4B
2.2	Latency	0.5	1.0	2.0	0.5	
2.3	Timing		1.0			
2.4	Synthesis areas		1.0	2.0		
2.5	Area Optimization	0.5			0.5	
2.6	Power					
2.7	Power optimization	0.5		2.0	0.5	
	Subtotals:	2.0	3.0	8.0	2.0	

TEACHING PRINCIPLES

This unit will be addressed from the strategy of project-oriented learning and deductive teaching method, allowing the consolidation of the following learning techniques: worksheet, documentary research, directed discussion, concept mapping, problem solving, and conduct additional issues of practice.

LEARNING EVALUATION

Diagnostic evaluation
Portfolio of evidence:

Worksheet	5%
Conceptual map	5%
Problems Handbook	10%
Teamwork	10%
Practice Reports	20%
Project Implementation	10%
Self-assessment rubrics	5%
Headings of co-evaluation	5%
Evidence of learning	30%

THEMATIC UNIT: III **TITLE:** FPGA Application Design

UNIT OF COMPETENCE

The student design hardware applications based on field programmable logic devices.

No.	CONTENTS	Teacher led-instruction HOURS		Autonomous Learning HOURS		REFERENCES KEY
		T	P	T	P	
3.1	Hierarchical design	0.5	1.0	2.0	0.5	6B
3.2	Behavioral-level design	0.5	1.0	2.0	0.5	
3.3	Level design data flow	0.5	1.0	2.0	0.5	
3.4	Gate level design	0.5	1.0	2.0	0.5	
	Subtotals:	2.0	4.0	8.0	2.0	

TEACHING PRINCIPLES

This unit will be addressed from the strategy of project-oriented learning and deductive teaching method, allowing the consolidation of the following learning techniques: worksheet, documentary research, directed discussion, concept mapping, problem solving , teamwork and complementary topics internships

LEARNING EVALUATION

Diagnostic evaluation
Portfolio of evidence:

Worksheet	5%
Conceptual map	5%
Problems Handbook	10%
Teamwork	10%
Practice Reports	20%
Project Implementation	10%
Self-assessment rubrics	5%
Headings of co-evaluation	5%
Evidence of learning	30%

THEMATIC UNIT: IV **TITLE:** Design simulation

UNIT OF COMPETENCE

The student simulates the operation of applications based on field programmable logic devices.

No.	CONTENTS	Teacher led-instruction HOURS		Autonomous Learning HOURS		REFERENCES KEY
		T	P	T	P	
4.1	Behavioral simulation	0.5	1.0	2.0	0.5	4B
4.2	Functional simulation	0.5	1.0	2.0	0.5	
4.3	Timing simulation	0.5	1.0	2.0	0.5	
4.4	Printed circuit level simulation	0.5	1.0	2.0	0.5	
	Subtotals:	2.0	4.0	8.0	2.0	

TEACHING PRINCIPLES

This unit will be addressed from the strategy of project-oriented learning and deductive teaching method, allowing the consolidation of the following learning techniques: brainstorming worksheet, documentary research, directed discussion, concept maps, problem solving, teamwork and conduct additional issues of practice.

LEARNING EVALUATION

Diagnostic evaluation
Portfolio of evidence:

Worksheet	5%
Conceptual map	5%
Problems Handbook	10%
Teamwork	10%
Practice Reports	20%
Project Implementation	10%
Self-assessment rubrics	5%
Headings of co-evaluation	5%
Evidence of learning	30%

THEMATIC UNIT: V **TITLE:** Synthesis and routing designs

UNIT OF COMPETENCE

The student designs hardware applications based on the optimization of processes and variables involved in the stages of synthesis and routing.

No.	CONTENTS	Teacher led-instruction HOURS		Autonomous Learning HOURS		REFERENCES KEY
		T	P	T	P	
5.1	Synthesis and design optimization	0.5	1.0	2.0	0.5	1B,2B
5.1.1	Logic synthesis					
5.1.2	Physical synthesis					
5.2	Partition designs with layers	0.5	1.0	2.0	0.5	
5.3	Optimization of layers	0.5		3.0	0.5	
5.4	Generation of constraints		1.0	2.0		
5.5	Reducing delays in routing	0.5	1.0	2.0	0.5	
	Subtotals:	2.0	4.0	11.0	2.0	

TEACHING PRINCIPLES

This unit will be addressed from the strategy of project-oriented learning and deductive teaching method, allowing the consolidation of the following learning techniques: brainstorming worksheet, documentary research, directed discussion, concept maps, problem solving, teamwork and conduct additional issues of practice.

LEARNING EVALUATION

Diagnostic evaluation
Portfolio of evidence:

Worksheet	5%
Conceptual map	5%
Problems Handbook	10%
Teamwork	10%
Practice Reports	20%
Project Implementation	10%
Self-assessment rubrics	5%
Headings of co-evaluation	5%
Evidence of learning	30%

THEMATIC UNIT: VI **TITLE:** Performance analysis and debugging

UNIT OF COMPETENCE

The student evaluates the operation of applications based on field programmable logic devices.

No.	CONTENTS	Teacher led-instruction HOURS		Autonomous Learning HOURS		REFERENCES KEY
		T	P	T	P	
6.1	Software testing	0.5	1.0	2.0	1.0	3B,4B
6.2	Hardware testing	0.5	1.0	3.0	1.0	
6.2.1	Test protocols and configuration					
6.2.2	Board-level testing					
	Subtotals:	1.0	2.0	5.0	2.0	

TEACHING PRINCIPLES

This unit will be addressed from the strategy of project-oriented learning and deductive teaching method, allowing the consolidation of the following learning techniques: brainstorming worksheet, documentary research, directed discussion, concept maps, problem solving, teamwork and conduct additional issues of practice.

LEARNING EVALUATION

Diagnostic evaluation
Portfolio of evidence:

Worksheet	5%
Conceptual map	5%
Problems Handbook	10%
Teamwork	10%
Practice Reports	20%
Project Implementation	10%
Self-assessment rubrics	5%
Headings of co-evaluation	5%
Evidence of learning	30%

RECORD OF PRACTICALS

No.	NAME OF THE PRACTICAL	THEMATIC UNITS	DURATION	ACCOMPLISHMENT LOCATION
1	Examples of basic designs	II	5.0	Digital Electronics Laboratory of the ESCOM-IPN.
2	Floating Point Unit	III	6.0	
3	Asynchronous Receiver Transmitter Unit	IV	6.0	
4	PS2-Keyboard Interface	V	6.0	
5	PS2-Mouse interface	VI	4.0	
		TOTAL OF HOURS	27.0	

EVALUATION AND PASSING REQUIREMENTS:

The practicals are considered mandatory to pass this learning unit.
The practicals worth 20% in each thematic unit.

PERIOD	UNIT	EVALUATION TERMS
1	I y II	Continuous evaluation 70% and written learning evidence 30%
2	III y IV	Continuous evaluation 80% and written learning evidence 20%
3	V y VI	Continuous evaluation 90% and written learning evidence 10% The learning unit I is 5% worth of the final score The learning unit II is 18% worth of the final score The learning unit III is 18% worth of the final score The learning unit IV is 22% worth of the final score The learning unit V is 27% worth of the final score The learning unit VI is 10% worth of the final score Other means to pass this Unit of Learning: • Evaluation of previously acquired knowledge, with base in the issues defined by the academy. • Official recognition by either another Academic Unit of the IPN or by a national or international external academic institution besides IPN.

KEY	B	C	REFERENCES
1	X		Cofer, R.C. (2006). Rapid System Prototyping with FPGAs, Accelerating the Design Process. UK: Elsevier-Newnes. ISBN: 978-0-7506-7866-7.
2	X		Deschamps, J. P. (2006). Synthesys of Arithmetic Circuits FPGA, ASIC, and Embedded Systems. New Jersey: John Wiley & Sons, Inc. ISBN: 978-0471-68783-2.
3	X		Ion, G. (2008). Digital Systems Design with FPGAS, UK: Elsevier-Newnes. ISBN-13: 978-0-7506-8397-5.
4	X		Kilts, S. (2007). Advanced FPGA Design Architecture, Implementation, and Optimization. New Jersey: John Wiley & Sons, Inc. ISBN 978-0-470-05437-6.
5	X		Parnell, K. (2003). Programmable Logic Design Quick Start Handbook. USA: Xilinx Inc. PN 0402205 Rev. 3, 10/03.
6	X		Pong, P. C. (2008). FPGA Prototyping by VHDL examples. New Jersey: John Wiley & Sons, Inc. ISBN: 978-0-471-72092-8.

INSTITUTO POLITÉCNICO NACIONAL

SECRETARÍA ACADÉMICA

DIRECCIÓN DE EDUCACIÓN SUPERIOR

TEACHER EDUCATIONAL PROFILE PER LEARNING UNIT

1. GENERAL INFORMATION

ACADEMIC UNIT: Escuela Superior de Cómputo.

ACADEMIC PROGRAM: Ingeniería en Sistemas Computacionales. **LEVEL** III

FORMATION AREA:

Institutional	Basic Scientific	Professional	Terminal and Integration

ACADEMY: Sistemas Digitales. **LEARNING UNIT:** Advanced FPGA Devices Programming.

SPECIALTY AND ACADEMIC REQUIRED LEVEL: Masters Degree or Doctor in Computer Science.

2. AIM OF THE LEARNING UNIT:
The student implements advanced digital circuits based on field programmable logic devices.

3. PROFFESSOR EDUCATIONAL PROFILE:

KNOWLEDGE	PROFESSIONAL EXPERIENCE	ABILITIES	APTITUDES
• Design of Digital Systems • Computer Architecture • Microprocessors and microcontrollers • One or more hardware description languages • Knowledge of the Institutional Educational Model. • English Spoken.	• One year experience in the industry (preferred, not essential). • One year experience in courses in digital system design • Two year experience in managing groups and collaborative work. • One year experience as a Professor of Higher Education.	• Analysis and synthesis. • Problems resolution. • Cooperative. • Leadership. • Applications of Institutional Educational Model. • Decision making.	• Responsible. • Tolerant. • Honest. • Respectful. • Collaborative. • Participative. • Interested to learning. • Assertive.

DESIGNED BY	REVISED BY	AUTHORIZED BY
M. en C. Miguel Ángel Vivanco **COORDINATING PROFESOR**	Dr. Flavio Arturo Sánchez Garfias Subdirector Académico	Ing. Apolinar Francisco Cruz Lázaro Director
Dr. Julio Cesar Sosa Savedra. M. en C. Víctor Hugo García Ortega. Dr. Mario Aldape Pérez. **COLLABORATING PROFESSORS**		

Date: 2012